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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,190	12/30/2003	Carlos J. Gonzalez	SNDK.334US0	9150

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PARSONS HSUE & DE RUNTZ LLP
595 MARKET STREET
SUITE 1900
SAN FRANCISCO, CA 94105

EXAMINER	
LI, ZHUO H	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 09/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/750,190	GONZALEZ ET AL.	
	Examiner	Art Unit	
	Zhuo H. Li	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) *1-7 and 13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *see office action*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of Group III (claims 8-12) in the reply filed on September 11, 2006 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

2. This application contains claims 1-7 and 13 drawn to an invention nonelected with traverse in reply filed on September 11, 2006. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

3. Accordingly, this Office action is in responds to the reply file on September 11, 2006, claims 8-12 are pending in the application.

Information Disclosure Statement

4. The Information Disclosure Statements filed on 06/21/2004 and 10/11/2005 has been considered.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 8-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Otake et al. (US Pub. 2004/0,030,825 hereinafter Otake).

Regarding claim 8, Otake discloses a method of operating a non-volatile memory system (1, figure 1) comprising operating the memory with data being written and read with each of at least a first degree of parallelism, i.e., two-block writing or four-block writing, (pages 2-3 [0036] to [0040]), and a second degree of parallelism, i.e., single-block writing, (page 3 [0041] to [0043]), observing data write requests received by the memory system, i.e., new data writing, or rewriting exiting data, and writing data accompanying individual ones of the received write requests with one of the at least first and second degrees of parallelism in response to at lest one characteristic of the received write requests (pages 4-5 [0066] to [0074]).

Regarding claim 9, Otake discloses the at least one characteristic includes an amount of data received with a write request to be written into the memory, i.e., either rewriting partial data, or all data, (pages 4-5 [0066] to [0074]).

7. Claims 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Mukaida et al. (US Pub. 2003/0,028,704 hereinafter Mukaida).

Regarding claim 10, Mukaida discloses a flash memory system (1, figure 1) having an array of non-volatile memory cells (2-0 to 2-3, figure 1 and pages 4-5, [0084] to [0085]), arranged in blocks as a unit of erase, pages therein as a unit of data programming and reading and planes of plurality of blocks are independently accessible (figure 4 and page 6 [0105] to [0108]), a method of operation comprising logically forming metablocks, i.e., virtual block, that individually include a block from a plurality of the planes (figure 6, page 7 [0116] to [0120]), sequentially receiving write commands with varying amounts of data, i.e., series write command with successive host addresses, (page 9 [0164]), and variously writing the received data in parallel either sequentially into pages within individual blocks of one of the planes (figure 12, and pages 10-11 [0180] to [0193]), or in parallel into pages within two or more blocks of one of the metablocks in response to varying characteristics of the host write command (figure 22, page 17 [0289] to [0297], and pages 20-20, [0345] to [0346]).

Regarding claim 11, Mukaida discloses the method further comprising writing an indication at the same time as the received data that identifies the blocks into which the data are being written in parallel (page 16, [0275] to [0278]).

Regarding claim 12, Mukaida discloses a non-volatile memory system (1, figure 1) having an array of memory cells organized into blocks of cells that are erasable together and which individually store a plurality of unit of data (2-0 to 2-3, figure 1 and pages 4-5, [0084] to [0085]), a method of responding to a series of write commands, i.e., successive host addresses, that individually designate a logical address, i.e., virtual block address, of one or more units of data to be written and which are accompanied by the designated one or more units of data being received sequentially (figure 6, page 7 [0116] to [0120]), comprising converting, i.e., translating,

the logical address of an individual write command into a physical address within one or more of the blocks of memory cells (page 7 [0123] to [0124]) that allow writing the accompanying one or more units of data in parallel wherein a number of said one or more blocks are selected for receiving said one or more units of data as a function of the number of units of data specified by at least one of the received series of write commands (page 17, [0283] to [0286] and [0296] to [0297]), the number of units of data specified by the received series of write command varying, i.e., writing in different number of units of data is based on the successive host addresses, and its control bit and corresponding virtual block information to determining the number of units of data to be written into as an example of writing operation II, a number of units of data writing to the same memory chip (32-0), because the requesting addresses which related the virtual address with its corresponding physical blocks are resided in the same memory chip (page 7, [0296] to [0297]), and another example of writing operation III, a number of units of data writing to different memory chips (32-2 and 32-3) and (page 20 [0345]), Mukaida further discloses writing the selected one or more units of data into the one ore more blocks in parallel (page 17 [0029] to [0027], and page 20 [0345] to [0346]).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hasbun (US PAT. 5,541,886) discloses method and apparatus for storing control information in multi-bit non-volatile memory arrays (abstract).

Lakhani et al. (US PAT. 6,507,885) discloses memory system, method and pre-decoding circuit operable in different modes for selectively accessing multiple blocks of memory cells for simultaneous writing or erasure (col. 8 lines 9-63).

Sukegawa (US PAT. 5,572,466) discloses flash memory chip comprising an address conversion table as address conversion information, , and the flash memory chips are simultaneously accessed when a host designates the consecutive sector numbers for the same track (abstract).

Farmwald et al. (US PAT. 6,598,171) discloses integrated circuit input/output using a high performance bus interface, wherein the integrated circuit includes a protocol for master and salve devices to communicate on the bus and for registers in each device to differentiate each device and allow bus requests to be directed to a single or to all devices (abstract).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H. Li whose telephone number is 571-272-4183. The examiner can normally be reached on Tues - Fri 9:00am - 6:30pm and alternate Monday..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on 571-272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Zhuo H. Li

Patent Examiner
September 15, 2006

SANJIV SHAH
PRIMARY EXAMINER